(rather than claim 7) under §103 over the Johnson/Culley combination. This would seem to be more in consistence with the arguments made on pages 2 and 3 of the outstanding Official Action, as the Examiner does not appear to address dependent claim 7 requiring that the claim 1 invention is a "system-on-chip integrated circuit." Applicants will treat the rejection in section 3 as being a rejection of independent claims 1 and 8.

The Court of Appeals for the Federal Circuit, in the case of *In re Fine*, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988), held that "the PTO has the burden under §103 to establish a *prima facie* case of obviousness." The Court went on to say that the PTO "can satisfy this burden only by showing some objective teaching in the prior art . . . ." Thus, in order to support a rejection of claims 1 and 7, the cited prior art references must teach the structure recited in Applicants' independent claims.

Independent apparatus claim 1 and method claim 8 both recite that the data processing circuit is

> switchable between a first state in which said diagnostic interface circuit cannot perform at least some diagnostic operations upon said data processing circuit and a second state in which said diagnostic interface circuit can perform said at least some diagnostic operations upon said data processing circuit.

Thus, in order to support the rejection of independent claims 1 and 8 under 35 USC §103, the burden is on the Examiner to establish where at least one of the Johnson and Culley references disclose the claimed subject matter, i.e., the specified "data processing circuit." The Examiner clearly fails to meet his burden of proof, in that he not only fails to properly quote the recited subject matter from claims 1 and 8, he also identifies no portion of any reference by column and line number or figure number which discloses this apparatus structure or method step.

Specifically, in the sentence bridging pages 2 and 3 of the outstanding Official Action, the Examiner alleges generally that the Johnson reference "teaches the data processing circuit being switchable between a first state and a second state where a diagnostic interface circuit can perform at least some diagnostic operations." The Examiner correctly notes that Johnson teaches a fault tolerant computer having redundant channels so that operation can continue if one of the channels fails and thus, as suggested by the Examiner, Johnson has first and second states. However, this is not what claims 1 and 8 say.

Applicants' independent claims 1 and 8 are more specific than merely reciting "first and second states." The claims specify "a first state in which said diagnostic interface circuit cannot perform at least some diagnostic operations upon said data processing circuit." Claims 1 and 8 also specify a "second state in which said diagnostic interface circuit can perform said at least some diagnostic operations upon said data processing circuit." The Examiner ignores these definitions of Applicants' specified first and second states (perhaps because they are not disclosed in the cited prior art).

There is no indication in the Johnson reference, nor does the Examiner identify any column and line number providing such an indication, of the claimed definition of the two states. Johnson merely switches between identical, redundant operational channels, both of which do the same thing. There is no suggestion in Johnson or any other reference of a first state in which the circuit "cannot perform" at least some diagnostic operations and a second state in which the circuit "can perform" at least some diagnostic operations.

Should the Examiner persist in his rejection of independent claims 1 and 8 over the Johnson reference, he is respectfully requested to point out specifically where the Johnson

reference teaches Applicants' first and second states as defined in the claims, i.e., states in which the diagnostic interface circuit cannot perform in one state and can perform in the other state. Additionally, should the Examiner contend this is disclosed in Johnson, he is respectfully requested to identify the column and line number of such disclosure, as Applicants simply find no disclosure of this alleged structure and method step in the Johnson reference.

Additionally, the Examiner also alleges that Johnson teaches network interface controllers which allow digital communication between the fault tolerant computer systems. While this allegation does represent what is taught at column 5, lines 43-46, the Examiner's subsequent conclusion that Johnson "thus teaches a diagnostic transaction request master" is incorrect. The cited portion of the Johnson reference has nothing to do with Applicants' claimed "diagnostic transaction request master circuit . . . operable to issue diagnostic transaction requests to said diagnostic interface circuit."

The Examiner's allegation is in error, because he apparently does not appreciate that in Johnson it is the computer systems, and not the diagnostic interface circuits, which communicate via the network interface controllers. The cited portion of Johnson specifies that "the network interface controllers 112 and 128 allow digital communication between the fault tolerant computer system 100 and other computers (not shown) . . . ." (Column 5, lines 44-46). The Examiner apparently admits that Johnson does not contain Applicants' claimed diagnostic transaction request master circuit in his statement "he [Johnson] does not explicitly disclose diagnostic interface circuit to return a diagnostic bus transaction error signal to the diagnostic transaction request master." The Examiner relies upon the Cully reference, column 1, lines

63-66, for this teaching. However, again, the Examiner misinterprets the teaching in the Culley reference.

Culley teaches monitoring bus transactions for various faults associated with the transactions, i.e., bus timeouts, refresh holdoffs, bus hangs, etc. It is important to understand that these faults that Culley monitors are not the diagnostic interface circuit being "responsive to a diagnostic transaction request" and positively returning a diagnostic bus transaction error signal representing a perfectly legal bus behavior which is well understood by the diagnostic transaction request master circuit. This is not the same as the Culley reference in which bus transactions are observed for faults in the bus transaction themselves. In the cited portion of the Culley reference at column 1, lines 62-64, "the fault detectors provide indications to the central manager to indicate faulty operation of the respective circuits."

Thus, the Examiner's suggestion that Culley somehow teaches the admittedly absent structure from Johnson, i.e., the diagnostic interface circuit as set out in claims 1 and 8 is simply erroneous. How or why the Examiner believes Culley supplies the admittedly missing teaching in Johnson is not seen and clarification requested. Specifically, the Examiner is requested to identify the column and line number of the Culley teaching which he believes teaches the claimed diagnostic interface circuit or the diagnostic transaction request master circuit.

Without a disclosure of Applicants' claimed diagnostic interface circuit and diagnostic transaction request master circuit and the claimed interconnection, the Johnson and Culley references cannot disclose or render obvious the subject matter of independent claims 1 and 8 and any further rejection thereunder is respectfully traversed.

Moreover, the Examiner fails to provide any "reason" or "motivation" for one of ordinary skill in the art to combine the Johnson and Culley references. Why one of ordinary skill in the art would pick and choose the claimed elements from the Johnson and Culley references (assuming that the Examiner can identify some teaching of those elements in the respective references) and then combine them in the manner of Applicants' claims is simply not seen. Again, when combining references, the burden is on the Examiner to provide some "reason" or "motivation" for the combination. Here, the Examiner merely sets out a conclusory statement that it would be obvious to combine the two references without providing the required reason or motivation.

Claims 2-6 and 8-14 stand rejected under 35 USC §103 as unpatentable over the Johnson/Culley combination, further in view of Sheikh (U.S. Patent 6,202,160). As noted above, Applicants presume that the first rejection was intended to be of independent claims 1 and 8 and therefore will presume this second rejection with respect to dependent claims to be with respect to claims 2-7 and 9-14. Inasmuch as this rejection depends upon the rejection over the Johnson/Culley combination, the above comments distinguishing independent claims 1 and 8 from the Johnson/Culley combination are herein incorporated by reference.

There is no indication by the Examiner that the Sheikh reference contains the disclosures missing from the Johnson and Culley references, i.e., Applicants' specified "diagnostic interface circuit" and "diagnostic transaction master request circuit." Therefore, even if Sheikh were combined with Johnson and Culley, it would not disclose or render obvious the subject matter of independent claims 1 and 8, let alone dependent claims 2-7 and 9-14.

Moreover, the Examiner provides no reason or motivation as to why one of ordinary skill in the art would combine Johnson with Culley and Sheikh. The Examiner's conclusory statement that it would be obvious to combine Sheikh with Johnson does not address why it would be obvious to combine Sheikh with Culley or combine Johnson into Sheikh. The Examiner simply must provide some reason or motivation for picking and choosing amongst the various references and then combining the teachings in the manner of Applicants' independent claims 1 and 8 and claims 2-7 and 9-14 dependent thereon. Absent any specific identification of a "reason" or "motivation" for combining the three references, any further rejection thereunder is respectfully traversed.

Having responded to all objections and rejections set forth in the outstanding Official Action, it is submitted that claims 1-14 are in condition for allowance and notice to that effect is respectfully solicited. In the event the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of the above claims, he is respectfully requested to contact Applicants' undersigned representative.

Respectfully submitted,

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